LogiCORE IP Multiply Accumulator v3.0

DS716 October 2, 2013 **Product Specification**

Introduction

The Xilinx® LogiCORE™ IP Multiply Accumulator core provides implementations of multiply-accumulate using DSP slices. It accepts two operands, a multiplier and a multiplicand, and produces a product (A*B=Prod) that is added/subtracted to the previous result (S=S+/-Prod). This product value can be loaded by asserting Bypass (S=Prod). The function can be pipelined. The Multiply Accumulator module operates on signed or unsigned data.

Features

- Supports twos complement-signed and unsigned operations
- Supports multiplier inputs ranging from 1 to 31 bits unsigned or 2 to 32 bits signed and an output width ranging from 1 to 79 bits unsigned or 2 to 80 bits signed
- Optional clock enable and synchronous clear
- Latency can be set for optimal speed or minimal pipelining

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq®-7000, Virtex®-7, Kintex®-7, Artix®-7
Supported User Interfaces	N/A
Provided with Core	
Documentation	Product Specification
Design Files	Netlist
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Encrypted VHDL
Tested Design Tools(2)	
Design Entry Tools	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis Tools	Vivado Synthesis
Support	
Provided by Xilinx, Inc.	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Pinout

Signal names for the core symbol are shown in Figure 1 and described in Table 1.

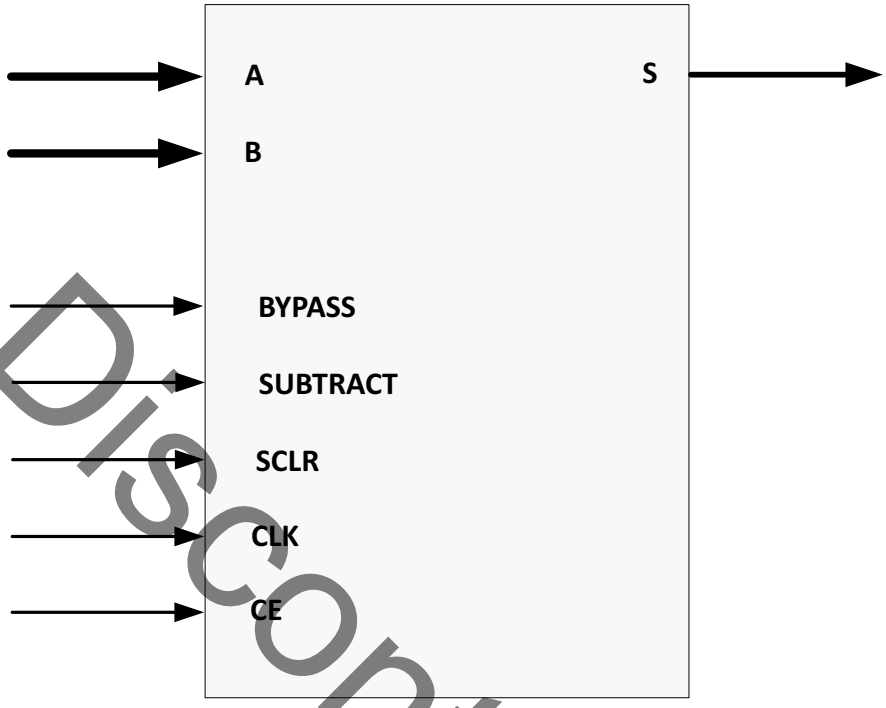

Figure 1: **Core Symbol**

Table 1: **Core Signal Pinout**

Name	Direction	Description
A[N:0]	Input	A Input bus (multiplier operand 1)
B[M:0]	Input	B Input bus (multiplier operand 2)
S[Q:0]	Output	Output bus
BYPASS	Input	Bypass Control Signal (Loads accumulator reg with product of A*B)
SUBTRACT	Input	Controls Add/Subtract operation (High = subtraction, Low = addition)
SCLR	Input	Synchronous Clear (active-High)
CLK	Input	Clock signal: rising edge
CE	Input	Clock Enable (active-High)

GUI Core Parameters

The core parameters for this module are described below:

- **Component Name**: The name of the core component to be instantiated. The name must begin with a letter and be composed of the following characters: a to z, 0 to 9, and "_".
- **A Input Width**: Sets the width of the Port A (multiplier operand 1) input. The valid range is 1 to 31 unsigned and 2 to 32 signed. The default value is 16.
- **B Input Width**: Sets the width of the Port B (multiplier operand 2) input. The valid range is 1 to 31 unsigned and 2 to 32 signed. The default value is 16.
- **A Input Type**: Sets the type of the Port A data: Signed, Unsigned. The default value is Signed.
- **B Input Type**: Sets the type of the Port B data. Signed, Unsigned. The default value is Signed.
- **Accumulation Width**: Sets the internal width of the accumulation function. The valid range is **A Input Width** + **B Input Width** + the number of "unsigned" inputs (0, 1, or 2) to 80. The default value is 48.
- **Output Width**: Sets the output width. The valid range is 2 to **Accumulation Width**. The default value is 16.
- **Accumulation Mode**: Sets the mode of operation of the module. Valid values are Add, Subtract, and Add-Subtract. If an adder/subtractor is specified, the SUBTRACT pin sets the mode of operation. The default is Add.
- **Bypass**: When set to true, creates a BYPASS pin. Activating the BYPASS pin sets the output to be the value given by the product of A and B. The default is for no BYPASS pin to be generated. The default value is false.
- **Bypass Sense**: Set to Active High or Active Low. The default value is Active High.
- **Synchronous Controls and Clock Enable (CE) Priority**: This parameter controls whether or not the SCLR input is qualified by CE. When set to "Sync Overrides CE", SCLR overrides the CE signal. When set to "CE Overrides Sync", SCLR has an effect only when CE is high. The default is "Sync Overrides CE".
- **Latency Configuration**: Automatic or Manual; Automatic sets optimal latency for maximum speed; Manual sets **Latency** to 1 or the *optimal value*. The default is Manual.
- **Latency**: Value used for latency when **Latency Configuration** is set to Manual: Two possible values are 1 (minimal latency) and *optimal latency*. See the section, Pipelined Operation for more information. The default value is 1.

Core Use through Vivado Design Suite

The IP GUI performs error-checking on all input parameters. Resource estimation and latency information are also available.

Several files are produced when a core is generated, and customized instantiation templates for Verilog and VHDL design flows are provided in the `.veo` and `.vho` files, respectively.

Simulation Models

Starting with Multipy Accumulator v3.0 (2013.3 version), behavioral simulation models have been replaced with IEEE P1735 Encrypted VHDL. The resulting model is bit and cycle accurate with the final netlist. For more information on simulation, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 1].

Pipelined Operation

The Multiply Accumulator module can be optionally pipelined to meet two conditions:

- to provide the *minimal* amount of latency allowed by the function. Achieved by setting:
  - **Latency Configuration** = Manual and **Latency** = 1
- to provide the *optimal* amount of latency allowed. This can be achieved in two ways:
  - **Latency Configuration** = Automatic or
  - **Latency Configuration** = Manual and **Latency** = *optimal value*

For minimal latency (Latency = 1), only accumulation registers are present.

If bypass is requested on a pipelined module, the bypass value appears on the outputs after the number of clock cycles, specified by the latency control.

Performance and Resource Utilization

Performance and resource numbers for the Multiply Accumulator are not available for v3.0 of the core. They will be provided in future updates.

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Known Issues

The master answer record for the Multiply Accumulator is AR 54509.

Ordering Information

This LogiCORE IP module is included at no additional cost with the Vivado Design Suite and is provided under the terms of the Xilinx End User License Agreement. To generate the core, use the Vivado IP catalog, which is part of the Vivado Design Suite.

Please contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

References

1. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
2. Multiply Accumulator product page
3. *Vivado Design Suite User Guide: Designing with IP* (UG896)

Revision History

Date	Version	Description of Revisions
04/24/2009	2.0	First customer release of Multiply Accumulator core.
03/01/2011	2.1	Added support for Virtex-7 and Kintex-7.
03/20/2013	3.0	Updated for core v3.0, and Vivado Design Suite-only support.
10/02/2013	3.0	Updated IP Facts table and Simulation Models information.

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