Programming & Debug Module Selection Guide

XILINX®

Xilinx Programming, Debug & Trace Products

Platform Cable USB II

Programming and Basic Debug

HW-USB-II-G

- Device configuration
- JTAG debugging
- Local programming and debug
- Simple driver development

SmartLynq Data Cable

Programming and Advanced Debug

HW-SMARTLYNQ-G

- Improved data-transfer and advanced debug
- Comparatively faster programming & JTAG debugging
- Remote debug capabilities
- OS aware debug
- System application development and debug (local or remote)

SmartLynq+ Module

Programming, High Speed Debug and Trace

HW-SMARTLYNQ-PLUS-G

- High speed debugging and trace data capture
- Serial and parallel trace support
- Reduced configuration time through HSDP
- In-depth debug capabilities for Versal™ architecture
- Software programmable built-in debugger
- Heterogeneous platform development and debug (local or remote)

Xilinx Debug Module: Resources

Comparison Metric	Platform Cable USB II	SmartLynq Data Cable	SmartLynq+ Module
Primary Target Device Family / Evaluation Kits	Cost-Optimized Portfolio	Zynq UltraScale+™ MPSoC and RFSoC	Versal™ ACAP
Target Connectivity	JTAG PC4	JTAG PC4, GPIO	JTAG PC4, GPIO, HSDP, Mictor(1)
Host Connectivity	-	USB 2.0, Ethernet	USB 3.0, Ethernet
Device Programming, HW/Basic SW Debug	Y	Y	Y
OS / Hypervisor Aware Debug	N	Y	Y
Maximum Theoretical Speed	24Mb/s (JTAG)	40Mb/s (JTAG)	10Gb/s (HSDP)
Measured Speed(2)	2.8Mb/s	3.1Mb/s	93.0Mb/s(3)
Time Taken to Load 100MB Linux	4:50 minutes	4:27 minutes	9 seconds (HSDP)
Trace Capability (Serial)	N	N	Y (Up to 10Gb/s per lane)
Trace Memory Size (Buffer)	–	–	Up to 14GB
Remote Access/Debug Capability	N	Y	Y
10/100/1000 Ethernet Host Interface	N	Y	Y
Default Bitstream Programming Speed (MB/s)	0.4	4	4
JTAG Max Clock Speed (MHz)	24	40	100
Connection to Target via PC4 JTAG or Flying Leads (provided)	Y	Y	Y
GPIO Available with Flying Leads Cable (provided)	N	Y	Y
Hardware Server Application	On Host	Local to Cable	Local to Cable

1. Currently not supported, reserved for future use
2. Speeds based on a single 2020.2 measurement downloading Linux
3. Difference in 2020.2 due to non-concurrent JTAG transactions, loose packing of HSDP transactions, and TCL overhead.