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Versal™ ACAP AI Edge Series Product Selection Guide

Industry's First Adaptive Compute Acceleration Platform (ACAP)

Versal™ AI Edge Series – Resources

		VE2002	VE2102	VE2202	VE2302	VE2602	VE1752	VE2802
Intelligent Engines	AI Engine-ML Tiles	8	12	24	34	152	0	304
	AI Engine Tiles	0	0	0	0	0	304	0
	AIE/AIE-ML Data Memory (Mb)	4	6	12	17	76	76	152
	AIE-ML Shared Memory (Mb)	48	48	68	68	304	0	304
	DSP Engines	90	176	324	464	984	1,312	1,312
Adaptable Engines	System Logic Cells	43,750	80,080	229,688	328,720	820,313	981,120	1,139,040
	LUTs	20,000	36,608	105,000	150,272	375,000	448,512	520,704
	NoC Master / NoC Slave Ports	2	2	5	5	21	21	21
	Distributed RAM (Mb)	0.6	1.1	3.2	4.6	11.4	13.7	15.9
Memory	Total Block RAM (Mb)	0.8	1.7	3.8	5.4	16.7	33.5	21.1
	UltraRAM (Mb)	6.8	13.2	30.4	43.6	63.0	129.9	74.3
	Accelerator RAM (Mb)	32	32	32	32	0	0	0
	Total PL Memory (Mb)	40.2	48	69.4	85.6	91.1	177.1	111.3
	DDR Memory Controllers	1	1	1	1	3	3	3
	DDR Bus Width	64	64	64	64	192	192	192
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC						
	Real-Time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory	256KB On-Chip Memory w/ECC						
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
Serial Transceivers	GTY Transceivers (32.75Gb/s)	0	0	0	0	0	44	0
	GTYP Transceivers (32.75Gb/s)	0	0	8	8	32	0	32
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	-	-	-	-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX
	PCI Express®	-	-	1 x Gen4x8	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	40G Multirate Ethernet MAC	0	0	1	1	2	2	2
	Video Decoder Engines (VDEs)	–	–	–	–	2	–	4
	Platform Mgmt Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug						

Versal AI Edge Series

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

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Versal™ AI Edge Series – Packages

			VE2002	VE2102	VE2202	VE2302	VE2602	VE1752	VE2802
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP						
SBVA484	19x19	0.8	84, 30 0, 78 0, 0	84, 30 0, 78 0, 0					
SBVA625	21x21	0.8	132, 84 0, 78 0, 0	132, 84 0, 78 0, 0					
SFVA784	23x23	0.8	132, 84 0, 78 0, 0	132, 84 0, 78 0, 0	132, 84 22, 78 0, 8	132, 84 22, 78 0, 8			
VSVG1369	35x35	0.92						132, 246 44, 78 24, 0	
VSVH1369	35x35	0.92					132, 192 44, 78 0, 32		132, 192 44, 78 0, 32
VSVA1596(1)	37.5x37.5	0.92						132, 246 44, 78 32, 0	
VFVH1760	40x40	0.92					186, 300 44, 78 0, 32		186, 300 44, 78 0, 32
VSVA2197	45x45	0.92						192, 294 44, 78 44, 0	

Versal AI Edge Series

Notes:
1. VE1752 in the VSVA1596 package supports LPDDR4 in 324 I/O only.

Versal™ AI Edge Series – Figures of Merit

			VE2002	VE2102	VE2202	VE2302	VE2602	VE1752	VE2802
Intelligent Engines	AI Engine Peak Perf – INT8x4	TOPs	11	16	32	45	202	101	405
	AI Engine Peak Perf – INT8	TOPs	5	8	16	23	101	101	202
	AI Engine Peak Perf – INT8x16	TOPs	3	4	11	11	101	51	101
	AI Engine Peak Perf – INT16	TOPs	1	2	4	6	25	25	51
	AI Engine Peak Perf – CINT16	Complex TOPs	0.2	0.2	0.5	0.7	3.2	6.3	6.3
	AI Engine Peak Perf – FP32	TFLOPs	0.4	0.7	1.3	1.9	8.3	6.3	16.6
	AI Engine Peak SRAM Bandwidth	Tb/s	11	16	32	45	202	405	405
	DSP Engine Peak Perf – INT8	TOPs	0.6	1.2	2.2	3.2	6.8	9.1	9.1
	DSP Engine Peak Perf – INT24	TOPs	0.2	0.4	0.7	1.1	2.3	3.0	3.0
	DSP Engine Peak Perf – CINT18	Complex TOPs	0.1	0.2	0.3	0.5	1.0	1.3	1.3
	DSP Engine Peak Perf – FP32	TFLOPs	0.1	0.3	0.5	0.7	1.6	2.1	2.1
Adaptable Engines	Adaptable Engine Peak Perf – INT1	TOPs	21	38	110	157	392	469	544
	Adaptable Engine Peak Perf – INT2	TOPs	10	18	50	72	180	215	250
	Adaptable Engine Peak Perf – INT4	TOPs	2	5	13	19	47	56	65
	Adaptable Engine Peak Perf – INT8	TOPs	1	1	3	5	12	14	17
	NoC Cross-sectional Bandwidth	Tb/s	0.6	0.6	0.6	0.6	1.7	1.7	1.7
Scalar Engines	Arm® Cortex-A72 Performance	DMIPs	15980	15980	15980	15980	15980	15980	15980
	Arm Cortex-R5F Performance	DMIPs	2505	2505	2505	2505	2505	2505	2505
Memory	Total Bandwidth - Block RAM	Tb/s	3	7	16	22	69	137	86
	Total Bandwidth - Ultra RAM	Tb/s	3	5	11	16	24	49	28
	Total Bandwidth - Accelerator RAM	Tb/s	0.4	0.4	0.4	0.4	0	0	0
	Total SRAM Bandwidth	Tb/s	6	12	27	39	92	186	114
	DDR4 Memory Bandwidth	Gb/s	25.6	25.6	25.6	25.6	76.8	76.8	76.8
	LPDDR4 Memory Bandwidth	Gb/s	34.1	34.1	34.1	34.1	102.4	102.4	102.4
I/O	Transceiver Bandwidth	Tb/s	0	0	0.52	0.52	2.10	2.88	2.10
	Sensor I/O Bandwidth	Gb/s	269	269	269	269	960	941	960

Versal AI Edge Series

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Versal™ ACAP Migration Table

Package Name	Footprint	Versal AI Edge Series							Versal AI Core Series							Versal Prime Series									Versal Premium Series						
		VE2002	VE2102	VE2202	VE2302	VE2602	VE1752	VE2802	VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802	VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902	VP1102	VP1202	VP1402	VP1502	VP1552	VP1702	VP1802
SBVA484	A484	■	■																												
SBVA625	A625	■	■																												
SFVA784	A784	■	■	■	■											■															
VBVA1024	A1024								■																						
NBVB1024	B1024																■	■													
VFVB1369	B1369																■	■	■												
VSVE1369	E1369								■																						
VSVF1369	F1369																■	■													
VSVG1369	G1369						■			■	■																				
VSVH1369	H1369					■		■						■	■																
VSVA1596(1)	A1596						■			■	■																				
VIVA1596(1)	A1596											■	■																		
VFVC1596	C1596																■	■													
VFVC1760	C1760																		■	■											
VSVD1760	D1760											■	■				■	■	■	■											
VFVF1760	F1760																				■	■	■	■	■	■	■				
VFVH1760	H1760					■		■						■	■																
VSVA2197	A2197						■			■	■	■	■						■	■											
VSVC2197	C2197																				■	■	■	■			■	■			
VSVA2785	A2785																									■	■	■	■	■	
VSVA3340	A3340																										■	■	■	■	
LSVC4072	C4072																													■	■

Legend
■ Device
— Migration Path

Note:
1. VSVA1596 package dimensions are 37.5x37.5mm, VIVA1596 package dimensions are 40x40mm with 1.25mm overhang

Versal™ ACAP Ordering Information

Device Name				Device Attributes				Package Definition			
XC	V	C	1902	-1	M	S	E	V	S	V	D1760
Xilinx XC: Commercial XA: Automotive XQ: Defense	**Architecture** Versal	**Series Name** E: AI Edge C: AI Core M: Prime P: Premium H: HBM	**Device Number** Digits 1-3: Value Identifier Digit 4: # of Primary Cores	**Speed Grade** -1: Slowest -2: Mid -3: Highest	**Voltage** L: Low (0.7V) M: Mid (0.80V) H: High (0.88V)	**Static Screen** S: Standard L: Low Static	**Temp Grade** E: 0 to 110°C(1) I: –40 to 110°C(1) Q: –40 to +125°C M: –55 to +125°C	**Ball Pitch** V: 0.92mm, w/LSC N: 0.92mm, no LSC S: 0.8mm L: 1.0mm	**Lid** S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring H: Lidded Overhang I: Lidless, w/Stiffener Ring & Overhang	**RoHS6 Code** (2) V: Pb-free Ball Q: Eutectic Ball R: Ruggedized, Eutectic Ball	**Footprint**

Note:
1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).
2. All packages have Pb-free bumps.