WP227 (v1.1) June 29, 2005

The Real Value of CoolRunner-II DataGATE

By: Mark Ng

DataGATE™ is a CoolRunner™-II CPLD feature that permits input signal blocking, stops input switching, and reduces power. DataGATE can block any input pins you select. Low power design can be attained without using DataGATE, but even greater results are possible for your entire design using it. With DataGATE, CoolRunner-II devices are the only CPLDs on the market that can quote a low standby current and have it actually mean something. This white paper will demonstrate the dramatic results that can be obtained for your design using DataGATE.

Introduction

No other CPLD approaches specified standby current without using external logic to block switching inputs. Adding external logic increases system power and cost. Data sheet statements about static current are simply incomplete, and potentially useless or dangerous. You cannot measure static current without external modification. This has little value, in real world circuits, except to state: *If all inputs were stopped, then current drawn would be X microamps.*

Unfortunately, for real world designs this statement has little meaning. To gain the benefits of low static current may require massive design changes. DataGATE gives you additional power reduction using no external resources.

How Good is DataGATE?

It's excellent! The results you get will depend on the design and how DataGATE is used. To clarify, we will provide guidelines for best results. Table 1 shows how much V_{CCINT} current is saved under various input blocking conditions. As shown in the first row of Table 1, the standby current (defined as the total amount of current drawn at 0 MHz) of this particular XC2C128 unit under test is 0.02 mA. Without DataGATE, current increases linearly as the number of inputs switching increase.

However, with DataGATE the CPLD can approach standby current without forcing all inputs to stop switching. DataGATE allows up to 99% power savings. Other CPLDs can try to specify a meaningless standby current, but CoolRunner-II is the only CPLD that can actually save power in a real world design, one that has actual inputs and outputs, and interacts with other devices.

V_{CCINT} Current Savings

The current savings on V_{CCINT} are substantial, as shown in Table 1.

Table 1: **Current Drawn on V_{CCINT} from Switching Inputs with/without DataGATE at 50 MHz.**

	Current Drawn on V_{CCINT} (mA)		
Inputs Switching	**No DataGATE**	**With DataGATE**	**Savings**
0	0.02	0.02	0%
1	0.82	0.02	97%
2	1.62	0.02	98%
3	3.09	0.02	99%
4	5.40	0.02	99%

Figure 1, Figure 2, Figure 3, and Figure 4 graphically show how V_{CCINT} current savings increase versus input signal frequency.

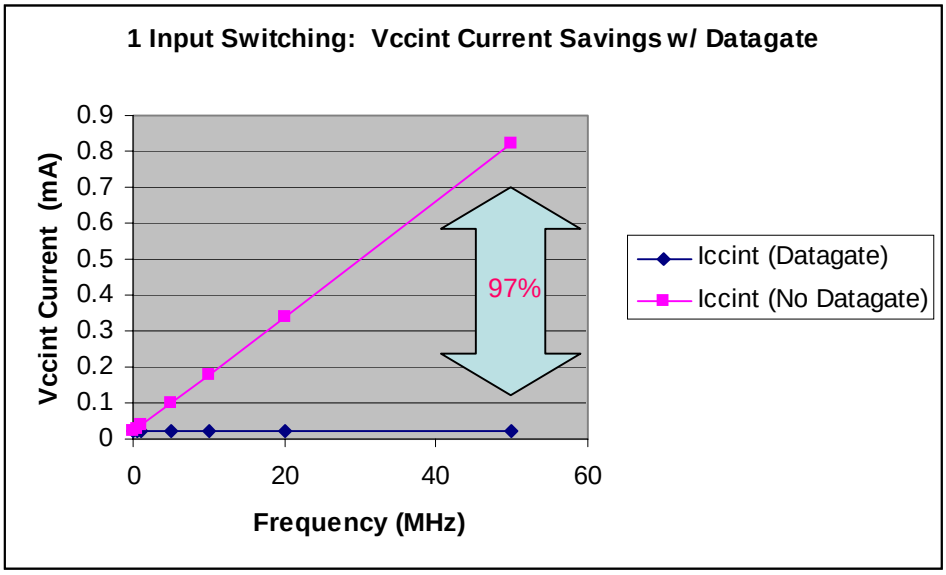

Figure 1: **V_{CCINT} Current Savings, Single Input Switching**

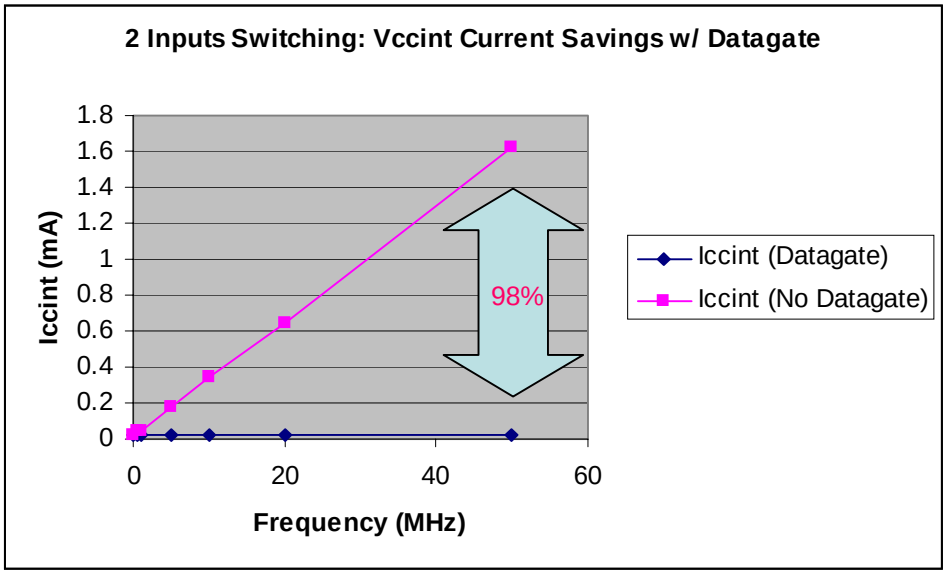

Figure 2: **V_{CCINT} Current Savings, Two Inputs Switching**

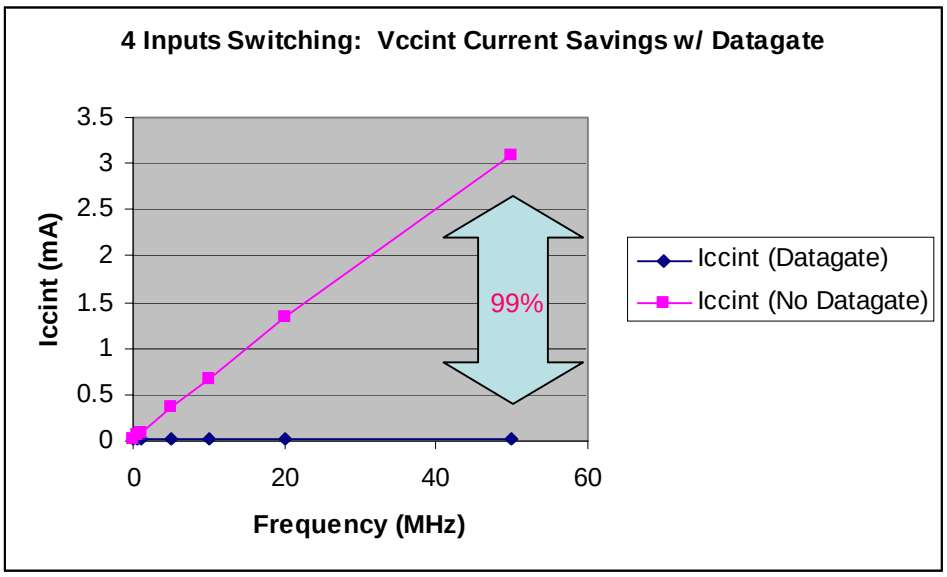

Figure 3: **V_{CCINT} Current Savings, Four Inputs Switching**

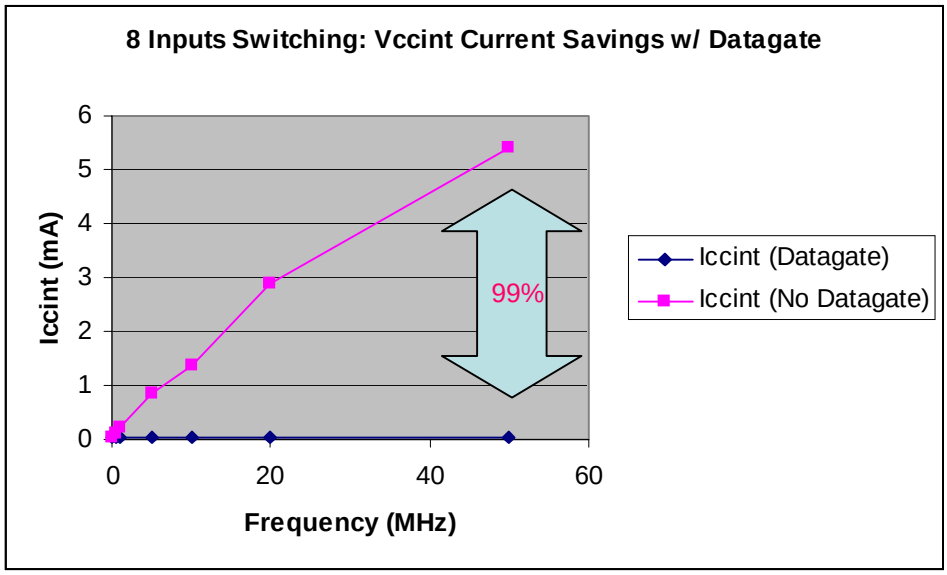

Figure 4: **V_{CCINT} Current Savings, Eight Inputs Switching**

What about V_{CCIO} Current?

At this point, we have established that a 'Standby Current' specification is relatively useless. No real design can operate with zero inputs toggling. We have also established that CoolRunner-II is the only CPLD in the world that allows a user to approach standby current without physically disconnecting all inputs. But all discussion thus far has concentrated on current drawn through the V_{CCINT} rail. What about current drawn through V_{CCIO}?

The entire industry avoids discussing current drawn through V_{CCIO}. No PLD manufacturer provides any specification whatsoever regarding how much current the I/Os will draw. Examine any CPLD data sheet. You will find that all I_{CC} versus Frequency graphs are specific to V_{CCINT} current. No reference is ever made to V_{CCIO}.

Why? This is primarily because current drawn through the I/Os is difficult for manufacturers to determine because it is dependent upon too many external variables (capacitive loading, frequency, current requirements, input rise time, and so on). In addition, as V_{CCIO} current can be significant (so significant that it can invalidate a device's low power message), most manufacturers have tended to avoid it.

Let's examine the effect of simply switching a few inputs. This time, instead of looking at V_{CCINT}, let's look at V_{CCIO}. How much current does that draw, and, can DataGATE do anything to reduce V_{CCIO} current?

Table 2: **Current Drawn on V_{CCIO} from Switching Inputs with/without DataGATE at 50 MHz**

	Current Drawn on V_{CCIO} (mA)		
Inputs Switching	**No DataGATE**	**With DataGATE**	**Savings**
0	0	0	0%
1	8.58	0.05	99%
2	14.86	0.11	99%
4	25.95	0.22	99%
8	43.82	0.44	99%

As can be seen in Table 2, this V_{CCIO} current can be quite large. However, with DataGATE asserted, the CoolRunner XC2C128 device can essentially shut down the internal I/O buffers and accomplish 99% power savings on the V_{CCIO} rail. Figure 5, Figure 6, Figure 7, and Figure 8 show V_{CCIO} current savings versus input switching frequency.

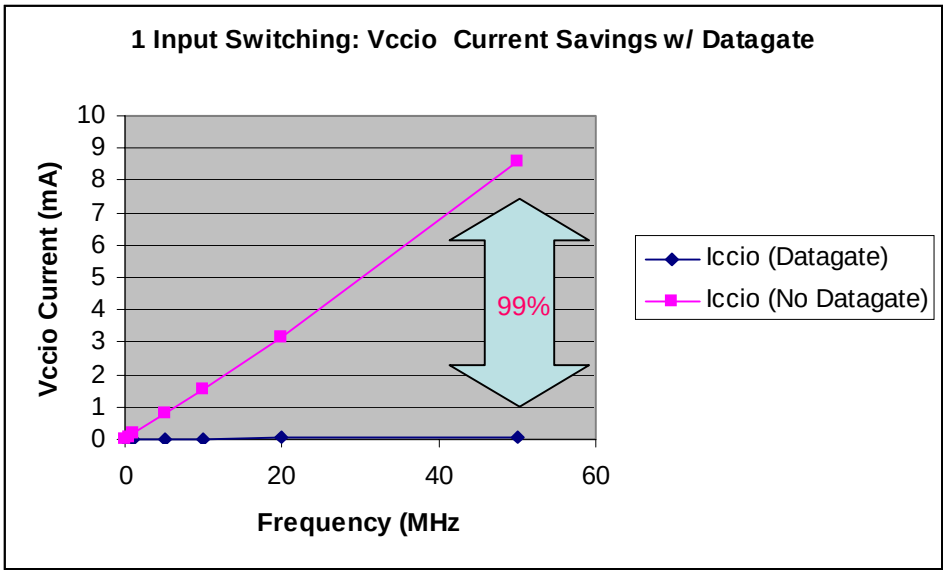

Figure 5: **V_{CCIO} Current Savings, Single Input Switching**

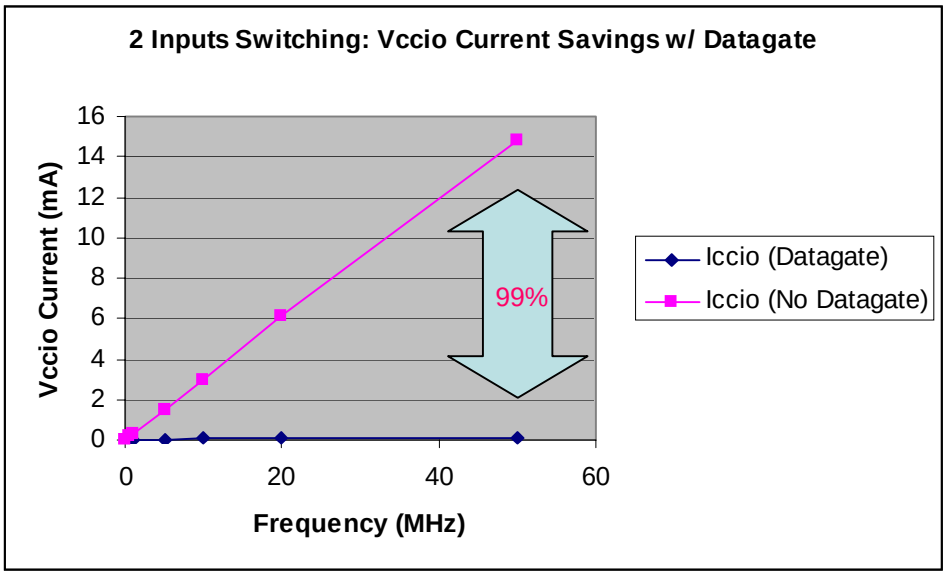

Figure 6: **V_{CCIO} Current Savings, Two Inputs Switching**

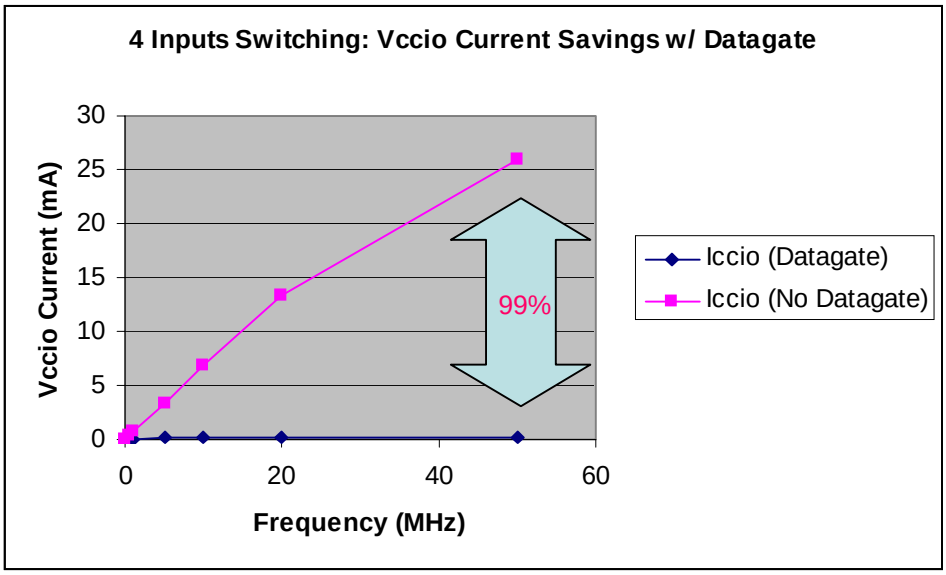

Figure 7: **V_{CCIO} Current Savings, Four Inputs Switching**

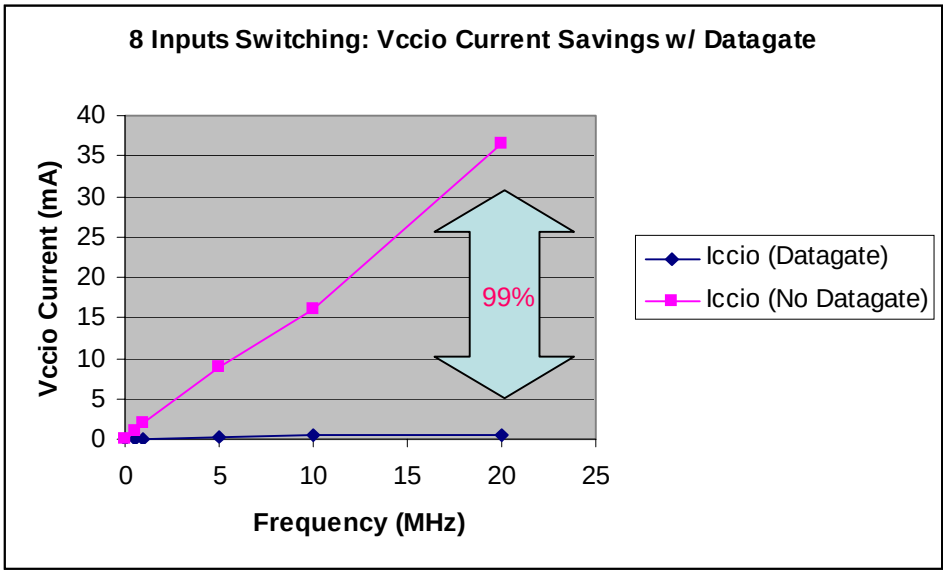

Figure 8: **V_{CCIO} Current Savings, Eight Inputs Switching**

We have already demonstrated one of the greatest kept secrets in the CPLD world -- although V_{CCINT} dynamic current can be quite low, V_{CCIO} current can exceed V_{CCINT} current by as much as 4x! It is no wonder that manufacturers do not specify V_{CCIO} current. Instead, they focus on what appears to be an extremely low standby current, which is basically useless. They focus on dynamic V_{CCINT} current, which is substantially less than V_{CCIO} current.

Other devices may appear to be low power, but only one device actually is low power. CoolRunner-II devices are the only CPLDs providing 99% savings on V_{CCINT} and 99% power savings on V_{CCIO}.

Conclusion

Table 1 and Table 2 understate the problem. Data was taken with simple buffers, showing the effect of blocking inputs into the chip. If those inputs connected to multiple sites within the CPLD, additional power would be drawn, driving the capacitance of the additional connections. Hence, the more complex the design, the more power is saved by blocking inputs. Because we cannot anticipate how much logic your inputs will drive, it is difficult to estimate how much current will be saved for a particular design. However, one thing is certain: CoolRunner-II is the leading low power device not only because it has low dynamic power consumption, but also because it is the only CPLD that allows a design to approach standby current during full operation.

Additional Resources

Xilinx has invested considerable time in developing the best ways to reduce power in digital systems that use our parts. The following documents give an idea of the many ways to approach the problem, so please become familiar with them as you select the methods that work best for you.

XAPP 395 describes how DataGATE works and outlines a general approach for reducing your power. Briefly, you simply create your design as you wish and measure your power (typically I_{CC}). Then, you identify signals that may be blocked, and redefine your design to block them with the DataGATE signal. You then measure your current and see if enough reduction occurs. If it works correctly and you wish to remove more current, block some more signals. Keep blocking and measuring to reduce current. If you block signals to the extent that the design no longer works, simply go back one step to the last point that worked. There are other approaches, but this one works well.

XAPP378 shows how to drive the design software to take advantage of the CoolRunner-II advanced features. DataGATE is one of many such features, as are advanced clocking (division, DualEDGE), Schmitt trigger inputs, and slew rate control.

XAPP436 shows how a CoolRunner-II CPLD can reduce power in other chips, along with the CPLD itself. This approach uses DataGATE to block switching signals that are not needed in the other chip, and contributes to the overall system power usage. If you are using CoolRunner-II as a level translator, you get DataGATE power management for free on devices of 128 macrocells and above. This application note explains how.

XAPP 377 shows a set of low power design practices, including DataGATE. There are many ways to reduce power, and Xilinx CPLDs show more ways to do that than any other competitor.

If you are not interested in measuring power, **XAPP 317** shows how to apply the CoolRunner-II power equation to arrive at a reasonable estimate of your application's power usage. Just working with the equation factors can provide insight into ways to reduce it, as well.

Finally, if you want to understand the deeper workings, **U.S. Patent #6,172,518** goes through the original approach for DataGATE. It was originally invented for the Xilinx XC9500/XL/XV family of CPLDs, but was only used in the CoolRunner-II Family, where dramatic power reduction would be most appreciated.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/30/05	1.0	Initial Xilinx release.
06/29/05	1.1	Web Publication